CLAIMS:

We claim:

1. A lead frame for a bottom lead type or lead end grid type semiconductor package comprising:

a rectangular or square paddle for mounting a semiconductor chip thereon;

a plurality of tie bars for supporting the paddle;

a plurality of leads arranged at each of four sides or two facing sides of the paddle in such a fashion that they are spaced apart from the associated side of the paddle while extending perpendicularly toward the associated side of the paddle, each of the leads having a lead lock adapted to increase a bonding force of the lead to a resin encapsulate subsequently to be molded thereon; and

dam bars for supporting the leads and the tie bars.

2. The lead frame in accordance with claim 1, wherein the paddle has a flat plate shape while having a partially etched structure at a peripheral portion thereof, and each of the tie bars has a partially etched portion.

3. The lead frame in accordance with claim 1, wherein each of the leads has an inverted-trapezoidal cross section in such a fashion that it has inclined side walls serving as the lead lock.

4. The lead frame in accordance with claim 1, wherein the lead lock of each lead comprises a partial etched portion formed at an inner end of the lead, the partial etched portion having an etched lower surface.

5. The lead frame in accordance with claim 1, wherein the lead lock of each lead comprises a partial etched portion formed at a portion of the lead outwardly spaced apart from an inner end of the lead, the partial etched portion having an etched upper or lower surface.

6. The lead frame in accordance with claim 1, wherein the lead lock of each lead comprises a bent inner end of the lead.

7. The lead frame in accordance with claim 1, wherein the lead lock of each lead comprises one or more elements selected from the group consisting of at least one locking lug, at least one disk-shaped protrusion, at least one dimple, at least one aperture, inclined side walls having an increased width defined therebetween in an upward direction, and a partially etched portion having an etched upper or lower surface.

8. A semiconductor package comprising:

a paddle;

a semiconductor chip mounted on the paddle by an adhesive layer interposed between the paddle and the semiconductor chip;

a plurality of leads arranged at each of four sides or two facing sides of the paddle in such a fashion that they are spaced apart from an adjacent side of the paddle while extending perpendicularly toward the adjacent side of the paddle, each of the leads having a lead lock;

conductive wires for electrically connecting respective inner ends of the leads to the semiconductor chip;

a resin encapsulate for encapsulating the semiconductor chip and the conductive wires; and

each of the leads having a lower surface exposed at the bottom of the resin encapsulate.

9. The semiconductor package in accordance with claim 8, wherein the lead lock of each lead comprises one or more elements selected from the group consisting of at least one locking lug, at least one disk-shaped protrusion, at least one dimple, at least one aperture, inclined side walls having an increased width defined therebetween in an

upward direction, a partially etched portion having an etched upper or lower surface, and a bent portion.

10. A semiconductor package comprising:

a paddle;

a plurality of leads arranged at each of four sides or two facing sides of the paddle in such a fashion that they are spaced apart from an adjacent side of the paddle while extending perpendicularly toward the adjacent side of the paddle, each of the leads having a protrusion at a lower surface thereof;

a semiconductor chip mounted on the paddle in such a fashion that a peripheral portion of the chip is arranged over an inner end of each of the leads;

electrical insulator layer between the leads and the semiconductor chip;

conductive wires for electrically connecting respective inner ends of the leads to the semiconductor chip; and

a resin encapsulate for encapsulating the semiconductor chip, the electrical insulator layer, and the conductive wires.

11. The semiconductor package in accordance with claim 10, further comprising:

a solder bar attached to a respective lower surface of each protrusion, each of the solder balls serving as an external input/output terminal.

12. The semiconductor package in accordance with claim 10, wherein each of the leads has lead lock.

13. The semiconductor package in accordance with claim 12, wherein the lead lock of each lead comprises one or more elements selected from the group consisting of at least one locking lug, at least one disk-shaped protrusion, at least one dimple, at least one aperture, inclined side walls having an increased width defined therebetween in an upward direction, a partially etched portion having an

etched upper or lower surface, and a bent portion.

14. The semiconductor package in accordance with claim 10, wherein:

a thermally-conductive adhesive layer is interposed between a lower surface of the semiconductor chip and an upper surface of the paddle; and

the electrical insulator layer comprises an insulating adhesive layer interposed between respective upper surfaces of the leads at respective inner end of the leads and the lower surface of the semiconductor chip at the peripheral portion of the semiconductor chip.

15. The semiconductor package in accordance with claim 10, wherein the electrical insulator layer is interposed between a lower surface of the semiconductor chip and an upper surface of the paddle and between respective upper surfaces of the leads at respective inner end of the leads and the lower surface of the semiconductor chip at the peripheral portion of the semiconductor chip.

16. The semiconductor package in accordance with claim 10, wherein:

the electrical insulator layer comprises an electrical insulating layer coated over the entire lower surface of the semiconductor chip; and

a thermally-conductive adhesive layer is interposed between the electrical insulator layer and an upper surface of the paddle.

17. The semiconductor package in accordance with claim 10, wherein the electrical insulator layer comprises an electrical insulating layer coated over the entire lower surface of the semiconductor chip while being in direct contact with an upper surface of the paddle and respective upper surfaces of the leads at respective inner ends of the leads.

18. A method for fabricating semiconductor packages by mounting semiconductor chips each having input/output pads on paddles of lead frame units included in a lead frame strip, each of the lead frame units having a plurality of leads each having an inner lead and an outer lead integral with each other, each of the semiconductor chips being arranged over the inner leads of the leads associated with the respective chip, the method comprising:

mounting each of the semiconductor chips on at least the upper surfaces of the inner leads associated therewith through a thermally-conductive electrically insulating layer;

a wire bonding an inner end of each inner lead to an associated one of input/output pads of the semiconductor chip via a conductive wire;

molding a resin encapsulate adapted to encapsulate the semiconductor chip, the conductive wires, the insulating layer, and the inner leads associated with the semiconductor chip while allowing each of the associated inner leads to have a portion exposed at the bottom of the resin encapsulate; and

cutting the outer leads of the lead frame strip around a periphery of the resin encapsulate so as to separate the leads.

19. The method in accordance with claim 18, further comprising:

24. The method in accordance with claim 23, further comprising:

attaching a solder ball to the irradiated lower surface of each of the protrusions.

25. The method in accordance with claim 23, wherein the laser beam forms a surface pattern on the protrusions, said surface pattern selected from the group consisting of a matrix pattern, a line pattern, a dot pattern, and a line/dot pattern.

26. The method in accordance with claim 23, further comprising:

plating the irradiated protrusions with at least one metal selected from gold, nickel, aluminum, and an alloy thereof.